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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,782	03/31/2004	Kiyoshi Mita	14225-049001 / F1040149US	5223
26211	7590	10/02/2006	EXAMINER	
FISH & RICHARDSON P.C. P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			CHU, CHRIS C	
			ART UNIT	PAPER NUMBER
			2815	

DATE MAILED: 10/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/813,782	Applicant(s) MITA, KIYOSHI	
	Examiner Chris C. Chu	Art Unit 2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 21 September 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 - 14 is/are pending in the application.
- 4a) Of the above claim(s) 4 and 5 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1 - 3 and 6 - 14 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
- ☒ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>9/21/06</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 21, 2006 has been entered. An action on the RCE follows.

Response to Amendment

2. Applicant's amendment filed on September 21, 2006 has been received and entered in the case.

Election/Restrictions

3. Claims 4 and 5 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected group II, there being no allowable generic or linking claim. Election was made without traverse in the reply filed on January 18, 2005.

It is suggested that applicants cancel claims 4 and 5 in response to this Office action.

Claim Objections

4. Claims 13 and 14 are objected to because of the following informalities:

(A) In claim 13, line 2, between “of the of the” insert --step portion--.

(B) In claim 14, line 2, between “of the of the” insert --step portion--.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1 – 3 and 6 – 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi (U. S. Pat. No. 6,107,679) in view of Higashi et al. (U. S. Pat. No. 5,918,113).

Regarding claims 1 and 6, Noguchi discloses in e.g., Fig. 7(c) a semiconductor device (the device in Fig. 7(c)), comprising:

- a mounting substrate (1; column 2, line 5) having a first main surface (the surface where the sealing resin 11 is formed) and a second main surface (the surface where the sealing resin 11 is not formed) opposite the first main surface (see Fig. 7(c)), wherein the mounting substrate (1) is a single layer (see Fig. 7(c));
- a step portion (19) in the mounting substrate (1), at a periphery of the first main surface (see Fig. 7(c)), wherein the step portion (19) extends to about the middle of the mounting substrate (1) in a thickness direction (see Fig. 7(c));

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- a first conductive pattern (3; column 2, lines 8 and 9) on the first main surface of the mounting substrate (1) located inside the step portion (see e.g., Fig. 7(c));
- a second conductive pattern (2; column 2, line 7) on the second main surface of the mounting substrate (see Fig. 7(c));
- a semiconductor element (8; column 2, line 16) fixed to the first main surface of the mounting substrate and electrically connected (by wire 10) to the first conductive pattern (3); and
- sealing resin (11; column 2, lines 38 and 39) covering the first main surface of the mounting substrate and the step portion to seal the semiconductor element (see Fig. 7(c)),
- wherein a side surface of the sealing resin (11) and a side surface of the mounting substrate (1) are located on a same plane (see Fig. 7(c)).

Noguchi discloses in e.g., Fig. 7(c) does not disclose the material of the mounting substrate being resin material (claims 1 and 6). Higashi et al. teaches in e.g., Fig. 1 the material of a mounting substrate (10) being resin material (column 2, lines 7 – 9). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the resin material of Higashi et al. as the specific material to form the mounting substrate of Noguchi as taught by Higashi et al. to provide a flexibility in the mounting substrate (column 2, lines 7 – 9).

Regarding claims 2 and 9, Noguchi discloses in e.g., Fig. 7(c) the first conductive pattern (3) comprising a bonding pad (the bonding area of 3 that is bonded to the wire 10) electrically connected to the semiconductor element (8) through a fine metallic wire (10) and a plating line

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(3) extending from the bonding pad to the step portion (since applicant does not specifically claim that the plating line extends toward the step portion and stops at the edge or periphery of the step portion, a reasonable interpretation of the term “extending” includes the structure taught by Noguchi). Furthermore, the term “plating” is a process designation, and would thus not carry patentable structure difference in this claim drawn to a product. See *In re Thorp*, 227 USPQ 964 (Fed. Cir. 1985).

Regarding claims 3 and 10, Noguchi discloses in e.g., Fig. 7(c) a plurality of the bonding pads (the bonding areas of 3 that are bonded to the wire 10) being arranged so as to surround the semiconductor element (8; see Fig. 7(c)), further comprising a wiring portion (the portion of the element 3 that is formed under the chip 8) extending from each of the plurality of bonding pads under the semiconductor element (see Fig. 7(c)).

Regarding claims 7 and 12, Noguchi discloses in e.g., Fig. 7(c) the second conductive pattern comprising electrodes (2) arranged in a matrix (see Fig. 7(C)).

Regarding claims 8 and 11, Noguchi discloses in e.g., Fig. 7(c) a semiconductor device (the device in Fig. 7(c)), comprising:

- a mounting substrate (1) having a first main surface (the surface where the sealing resin 11 is formed) and a second main surface (the surface where the sealing resin 11 is not formed) opposite the first main surface (see Fig. 7(c)), wherein the mounting substrate (1) is a single layer (see Fig. 7(c));
- a step portion (19) a periphery of the first main surface of the mounting substrate (1; see Fig. 7(c)), wherein the step portion (19) extends to about the middle of the mounting substrate (1) in a thickness direction (see Fig. 7(c));

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- a first conductive pattern (3) on the first main surface of the mounting substrate (1) located inside the step portion (see e.g., Fig. 7(c));
- a second conductive pattern (2) on the second main surface of the mounting substrate (see Fig. 7(c));
- a semiconductor element (8) fixed to the first main surface of the mounting substrate and electrically connected (by wire 10) to the first conductive pattern (3); and
- sealing resin (11) covering the first main surface of the mounting substrate and the step portion to seal the semiconductor element (see Fig. 7(c)),
- wherein an external side surface of the sealing resin (11) and a side surface of the mounting substrate (1) are located on a “substantially” same plane (see Fig. 7(c)).

Noguchi discloses in e.g., Fig. 7(c) does not disclose the material of the mounting substrate being resin material (claims 1 and 6). Higashi et al. teaches in e.g., Fig. 1 the material of a mounting substrate (10) being resin material (column 2, lines 7 – 9). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the resin material of Higashi et al. as the specific material to form the mounting substrate of Noguchi as taught by Higashi et al. to provide a flexibility in the mounting substrate (column 2, lines 7 – 9).

7. Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noguchi and Higashi et al. as applied to claims 1 and 8 above, and further in view of Patterson et al. (U. S. Pat. No. 4,843,188).

While Noguchi and Higashi et al. disclose the use of the first conductive pattern, Noguchi and Higashi et al. do not disclose the first conductive pattern extending laterally to the edge of the step portion of the first main surface. Patterson et al. teaches in e.g., Fig. 4 a first conductive pattern (418) extending laterally to the edge of a step portion (the step portion) of a first main surface (see e.g., Fig. 4). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the extension of the first conductive pattern of Patterson et al. extending to the edge of a step portion of the first main surface of Noguchi and Higashi et al. as taught by Patterson et al. to ensure the reliability by increase bonding area or to provide a testing area (column 2, lines 39 – 50).

Response to Arguments

8. Applicant's arguments with respect to claims 1 and 8 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724. The examiner can normally be reached on 11:30 - 8:00.

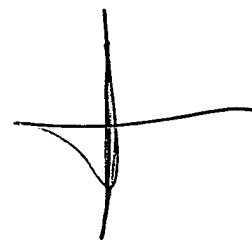
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Monday, September 25, 2006

A handwritten signature in black ink, appearing to read 'KENNETH PARKER', written over a horizontal line.

KENNETH PARKER
SUPERVISORY PATENT EXAMINER